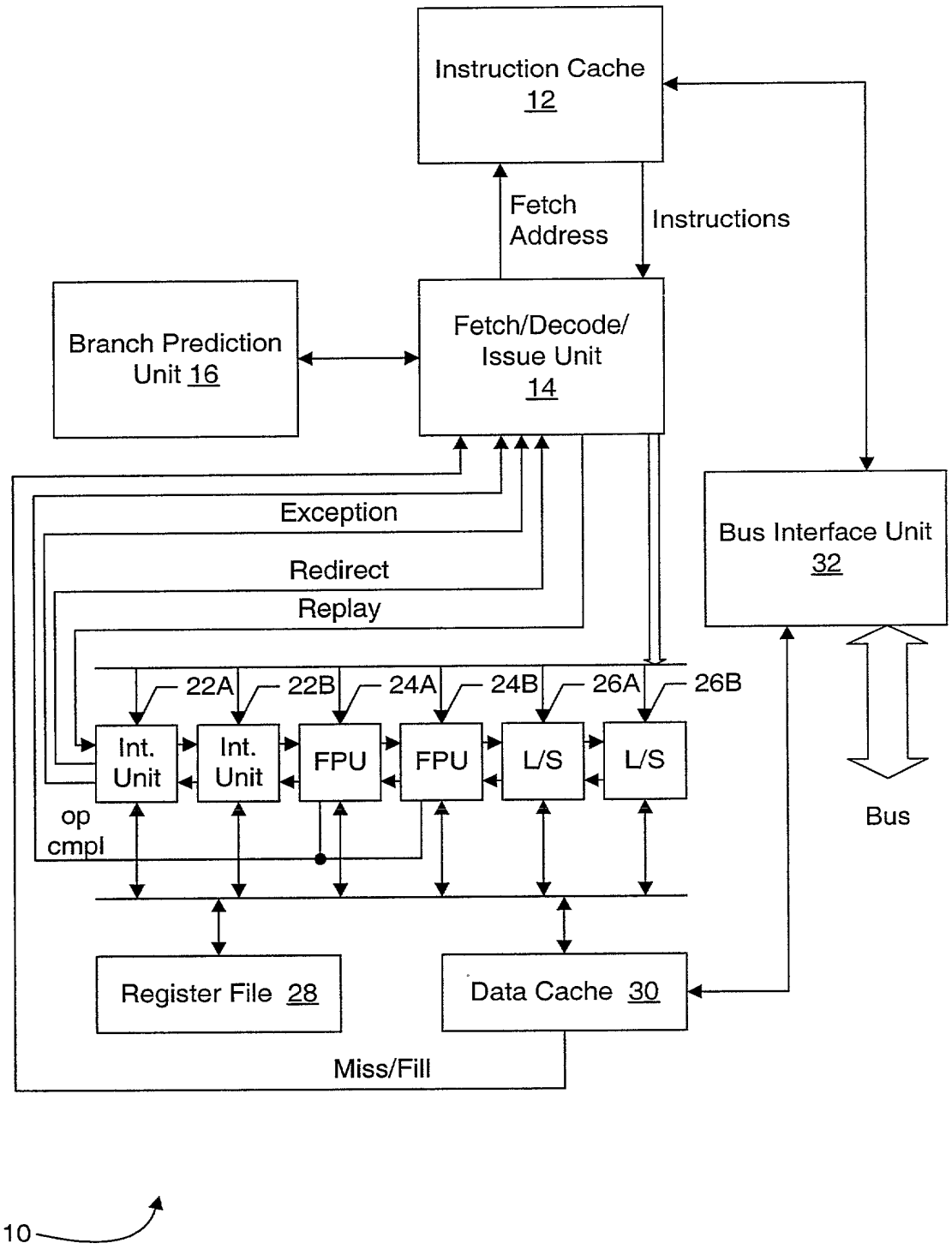
Instruction Cache
12
Fetch
Address
Instructions
Branch Prediction
Unit 16
Fetch/Decode/
Issue Unit
14
Exception
Redirect
Replay
Bus Interface Unit
32
22A
22B
24A
24B
26A
26B
Int.
Unit
Int.
Unit
FPU
FPU
L/S
L/S
op
cmpl
Bus
Register File 28
Data Cache 30
Miss/Fill
10

FIG. 1

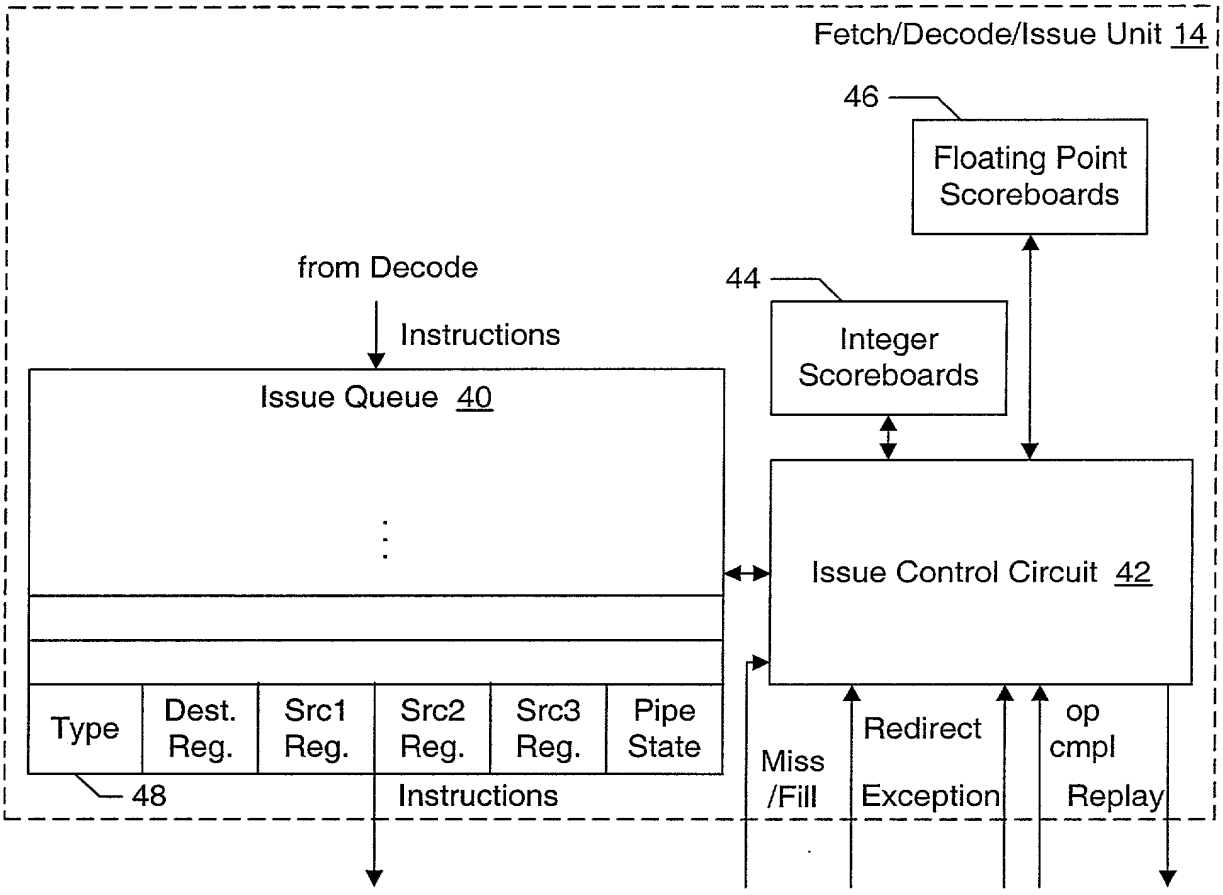
Fetch/Decode/Issue Unit 14
46
Floating Point Scoreboards
from Decode
Instructions
44
Integer Scoreboards
Issue Queue 40
Issue Control Circuit 42
Type
Dest. Reg.
Src1 Reg.
Src2 Reg.
Src3 Reg.
Pipe State
48
Instructions
Miss /Fill
Redirect
Exception
op cmpl
Replay
to Integer Units 22A-22B, FPUs 24A-24B, and L/S Units 26A-26B

FIG. 2

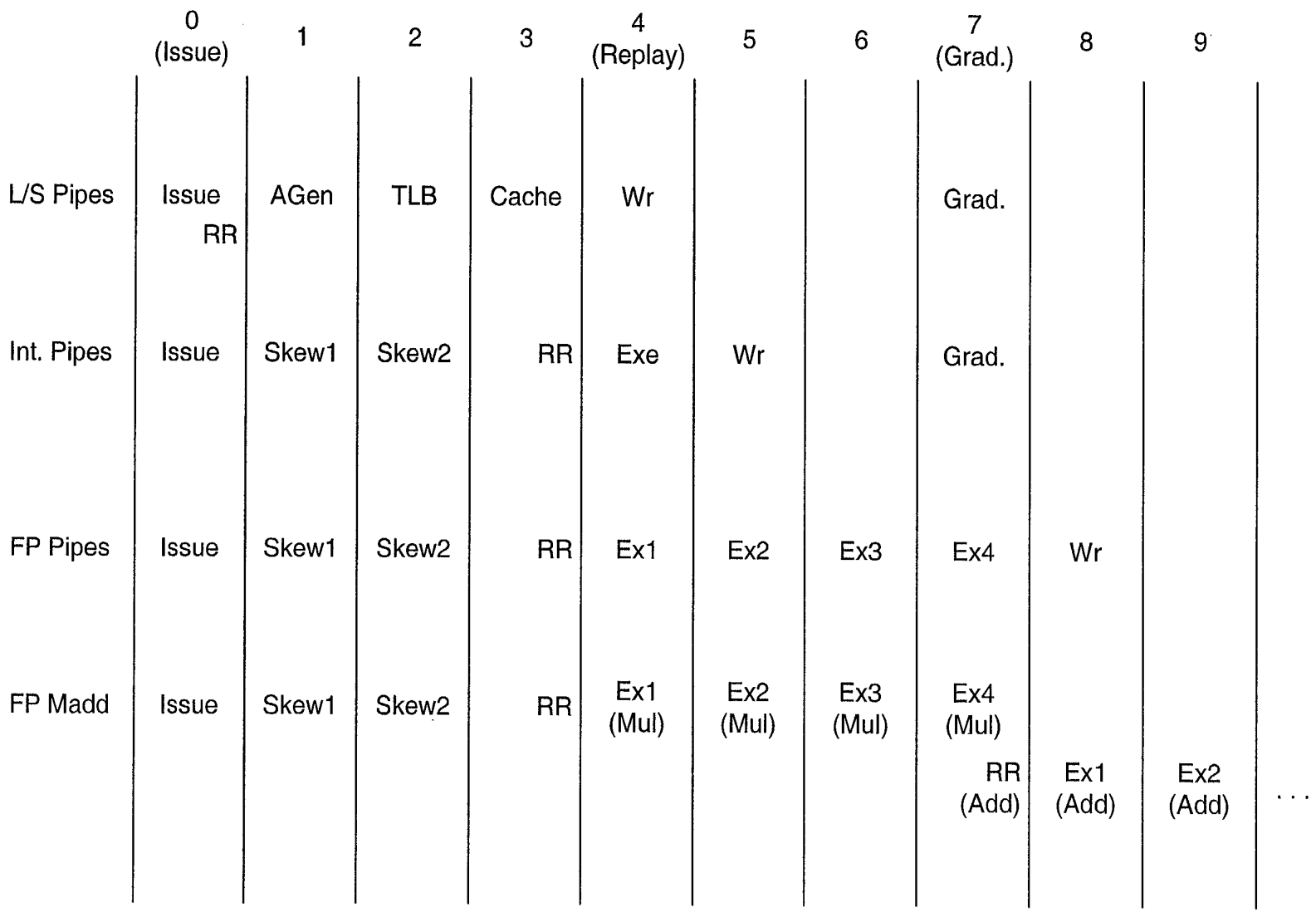
0 (Issue)
1
2
3
4 (Replay)
5
6
7 (Grad.)
8
9
L/S Pipes
Issue
RR
AGen
TLB
Cache
Wr
Grad.
Int. Pipes
Issue
Skew1
Skew2
RR
Exe
Wr
Grad.
FP Pipes
Issue
Skew1
Skew2
RR
Ex1
Ex2
Ex3
Ex4
Wr
FP Madd
Issue
Skew1
Skew2
RR
Ex1 (Mul)
Ex2 (Mul)
Ex3 (Mul)
Ex4 (Mul)
RR (Add)
Ex1 (Add)
Ex2 (Add)
. . .

FIG. 3

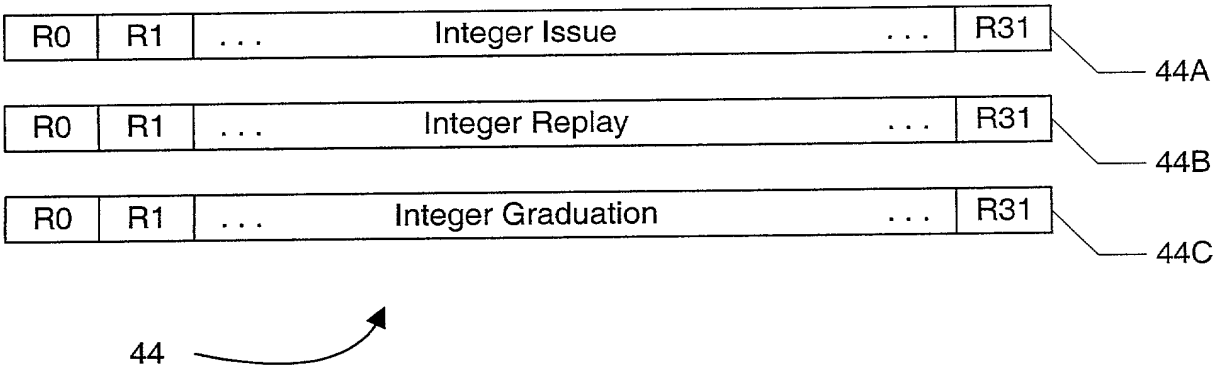
R0
R1
. . .
Integer Issue
. . .
R31
44A
R0
R1
. . .
Integer Replay
. . .
R31
44B
R0
R1
. . .
Integer Graduation
. . .
R31
44C
44

FIG. 4

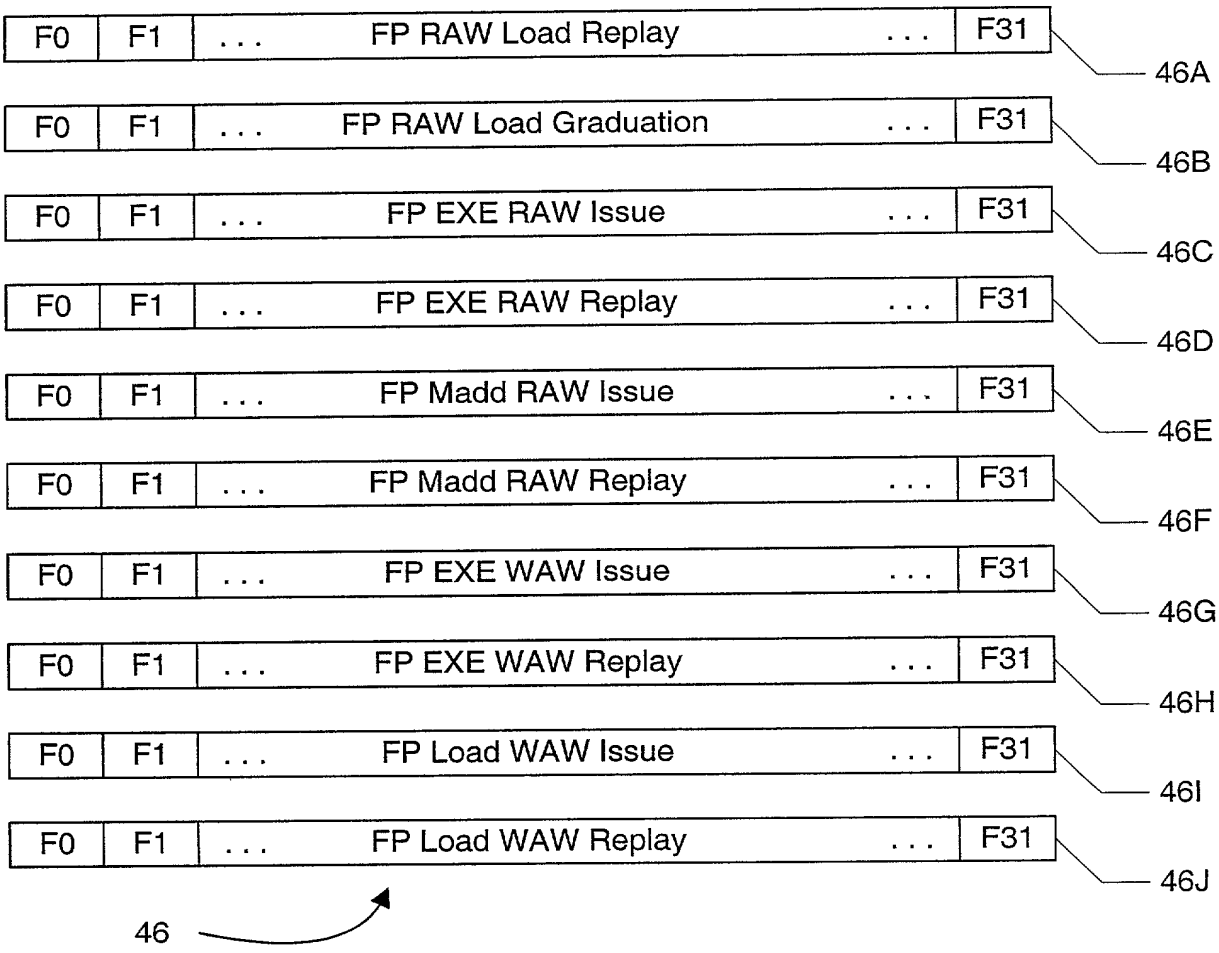
F0
F1
. . .
FP RAW Load Replay
. . .
F31
46A
F0
F1
. . .
FP RAW Load Graduation
. . .
F31
46B
F0
F1
. . .
FP EXE RAW Issue
. . .
F31
46C
F0
F1
. . .
FP EXE RAW Replay
. . .
F31
46D
F0
F1
. . .
FP Madd RAW Issue
. . .
F31
46E
F0
F1
. . .
FP Madd RAW Replay
. . .
F31
46F
F0
F1
. . .
FP EXE WAW Issue
. . .
F31
46G
F0
F1
. . .
FP EXE WAW Replay
. . .
F31
46H
F0
F1
. . .
FP Load WAW Issue
. . .
F31
46I
F0
F1
. . .
FP Load WAW Replay
. . .
F31
46J
46

FIG. 5

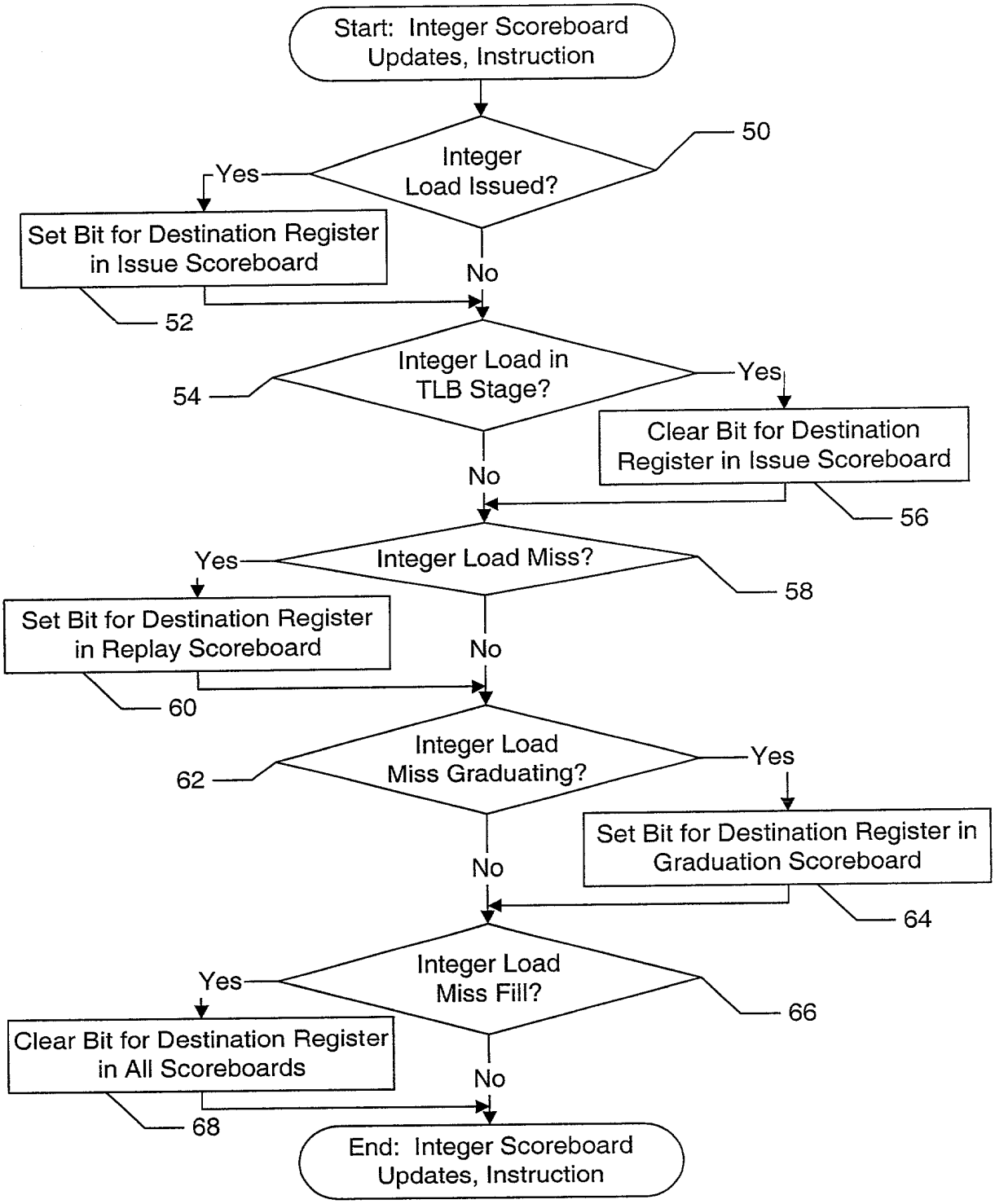
Start: Integer Scoreboard Updates, Instruction
Integer Load Issued?
50
Yes
Set Bit for Destination Register in Issue Scoreboard
52
No
Integer Load in TLB Stage?
54
Yes
Clear Bit for Destination Register in Issue Scoreboard
56
No
Integer Load Miss?
58
Yes
Set Bit for Destination Register in Replay Scoreboard
60
No
Integer Load Miss Graduating?
62
Yes
Set Bit for Destination Register in Graduation Scoreboard
64
No
Integer Load Miss Fill?
66
Yes
Clear Bit for Destination Register in All Scoreboards
68
No
End: Integer Scoreboard Updates, Instruction

FIG. 6

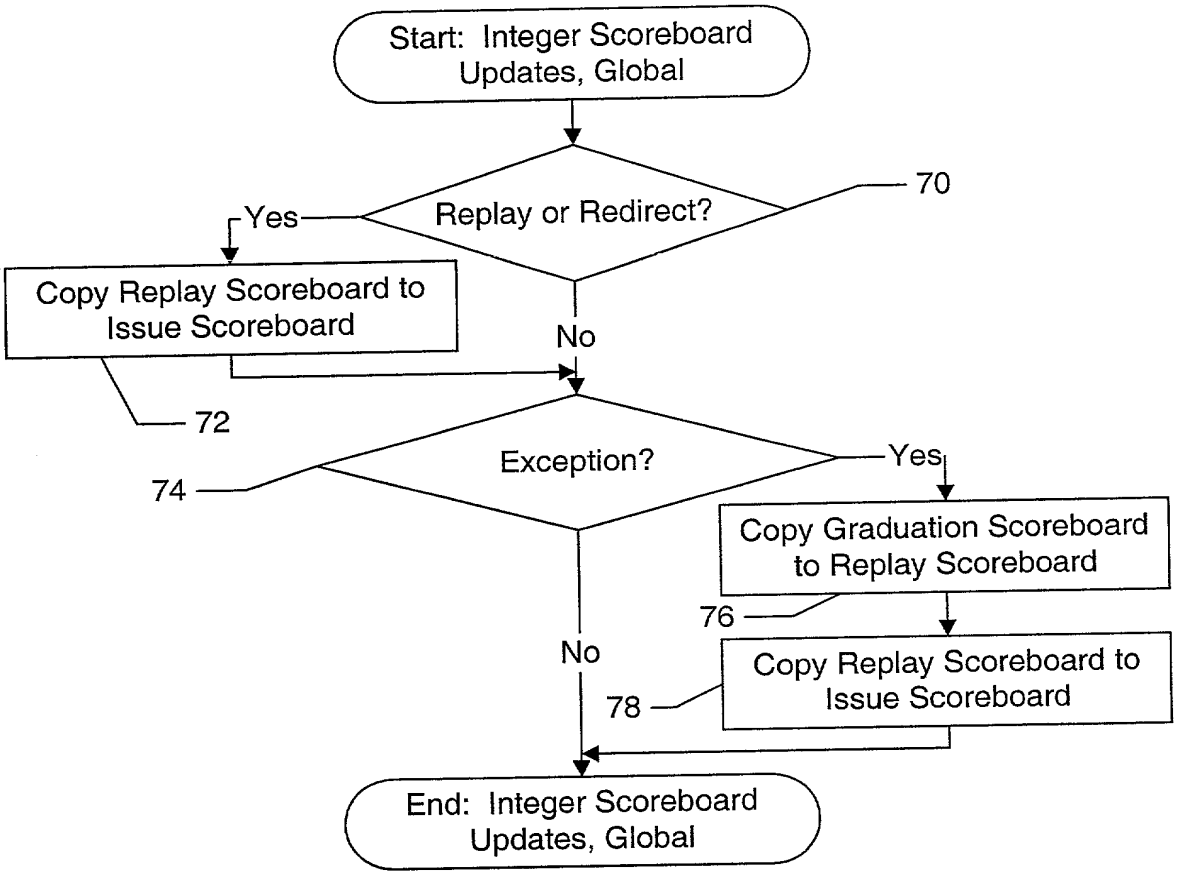
Start: Integer Scoreboard Updates, Global
Replay or Redirect?
70
Yes
Copy Replay Scoreboard to Issue Scoreboard
No
72
Exception?
74
Yes
Copy Graduation Scoreboard to Replay Scoreboard
76
No
Copy Replay Scoreboard to Issue Scoreboard
78
End: Integer Scoreboard Updates, Global

FIG. 7

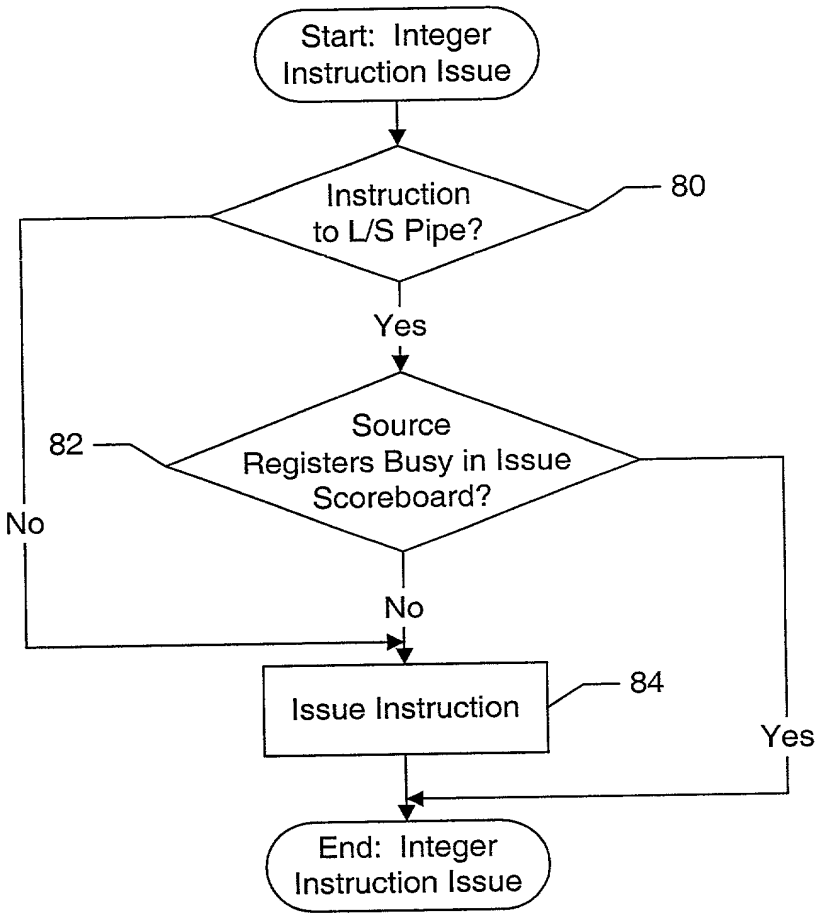
Start: Integer Instruction Issue
Instruction to L/S Pipe?
80
Yes
Source Registers Busy in Issue Scoreboard?
82
No
No
Issue Instruction
84
Yes
End: Integer Instruction Issue

FIG. 8

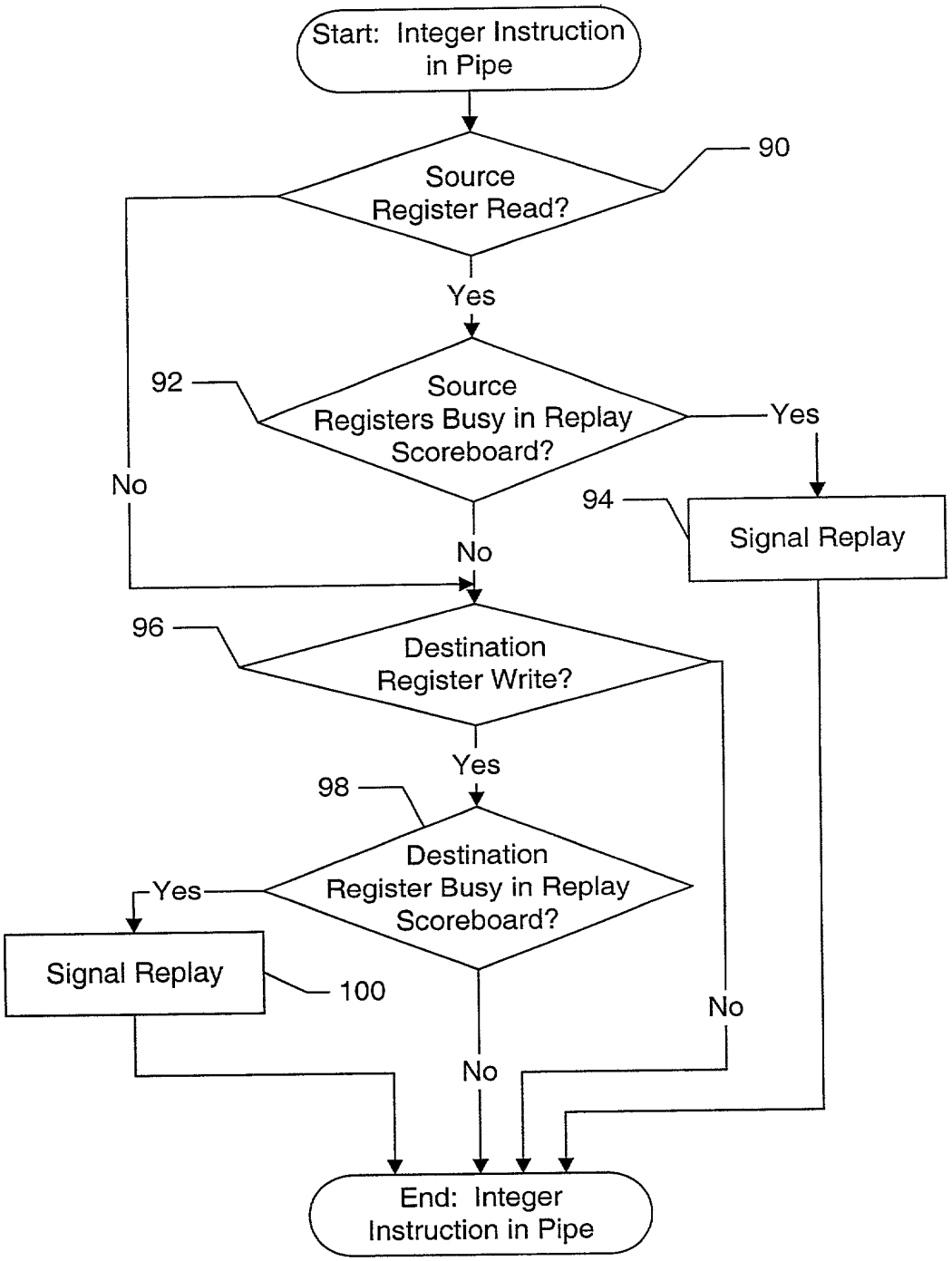
Start: Integer Instruction in Pipe
90
Source Register Read?
Yes
92
Source Registers Busy in Replay Scoreboard?
Yes
No
94
Signal Replay
No
96
Destination Register Write?
Yes
98
Destination Register Busy in Replay Scoreboard?
Yes
Signal Replay
100
No
No
End: Integer Instruction in Pipe

FIG. 9

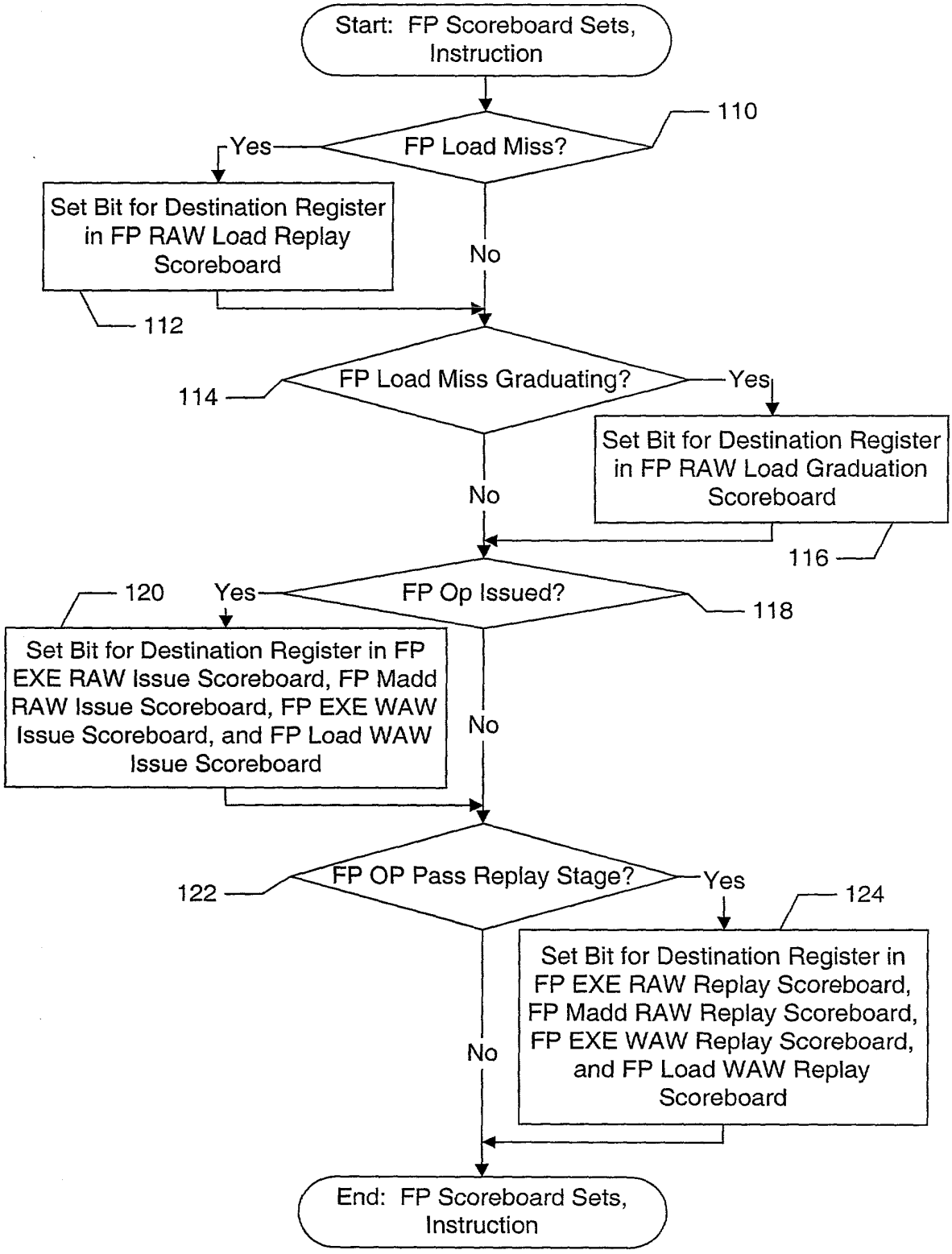
Start: FP Scoreboard Sets, Instruction
FP Load Miss?
110
Yes
No
Set Bit for Destination Register in FP RAW Load Replay Scoreboard
112
FP Load Miss Graduating?
114
Yes
No
Set Bit for Destination Register in FP RAW Load Graduation Scoreboard
116
FP Op Issued?
118
120
Yes
No
Set Bit for Destination Register in FP EXE RAW Issue Scoreboard, FP Madd RAW Issue Scoreboard, FP EXE WAW Issue Scoreboard, and FP Load WAW Issue Scoreboard
FP OP Pass Replay Stage?
122
Yes
No
124
Set Bit for Destination Register in FP EXE RAW Replay Scoreboard, FP Madd RAW Replay Scoreboard, FP EXE WAW Replay Scoreboard, and FP Load WAW Replay Scoreboard
End: FP Scoreboard Sets, Instruction

FIG. 10

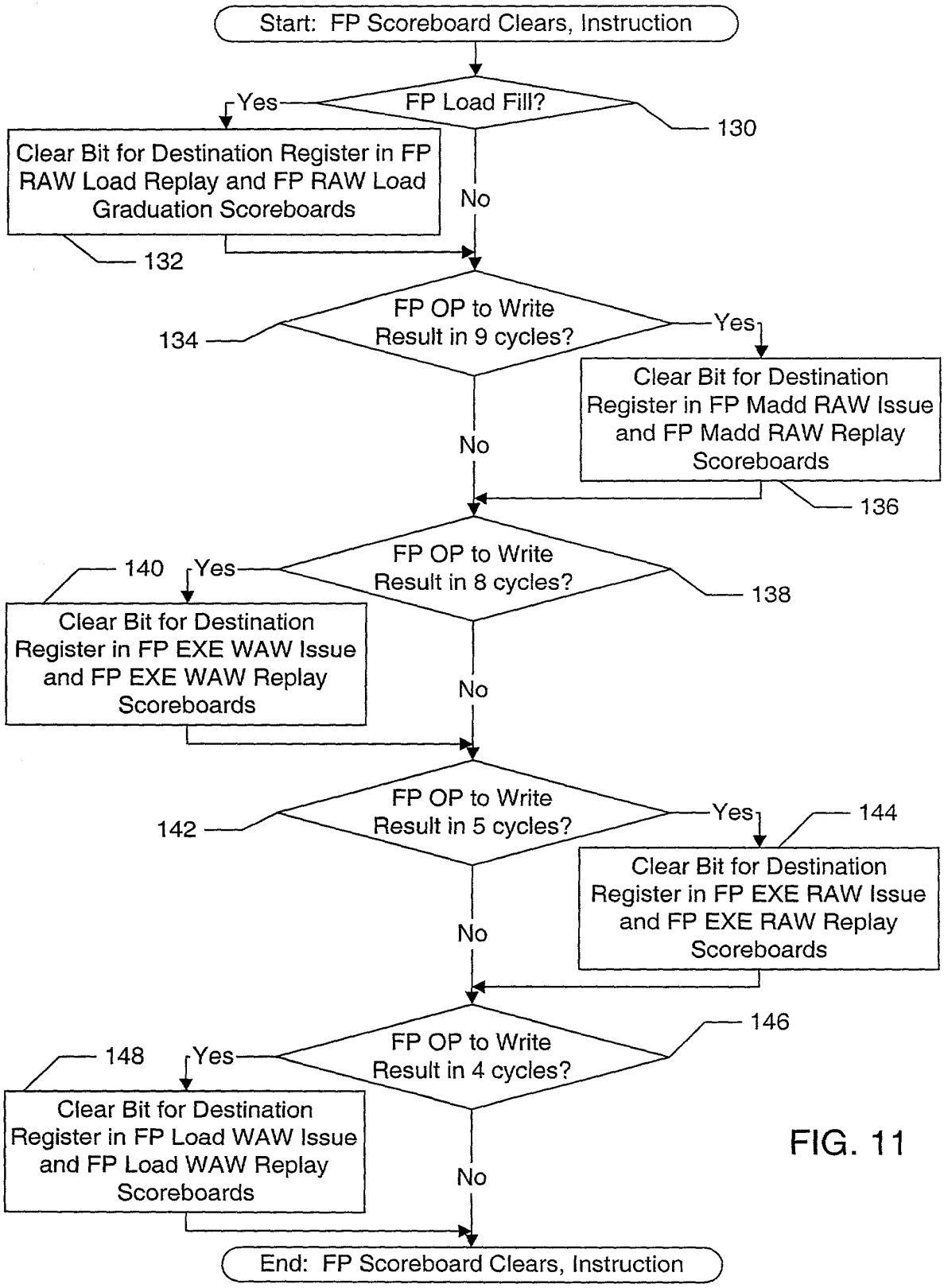
Start: FP Scoreboard Clears, Instruction
FP Load Fill?
Yes
130
Clear Bit for Destination Register in FP RAW Load Replay and FP RAW Load Graduation Scoreboards
132
No
FP OP to Write Result in 9 cycles?
134
Yes
Clear Bit for Destination Register in FP Madd RAW Issue and FP Madd RAW Replay Scoreboards
136
No
FP OP to Write Result in 8 cycles?
140
Yes
138
Clear Bit for Destination Register in FP EXE WAW Issue and FP EXE WAW Replay Scoreboards
No
FP OP to Write Result in 5 cycles?
142
Yes
144
Clear Bit for Destination Register in FP EXE RAW Issue and FP EXE RAW Replay Scoreboards
No
FP OP to Write Result in 4 cycles?
146
148
Yes
Clear Bit for Destination Register in FP Load WAW Issue and FP Load WAW Replay Scoreboards
No
End: FP Scoreboard Clears, Instruction

FIG. 11

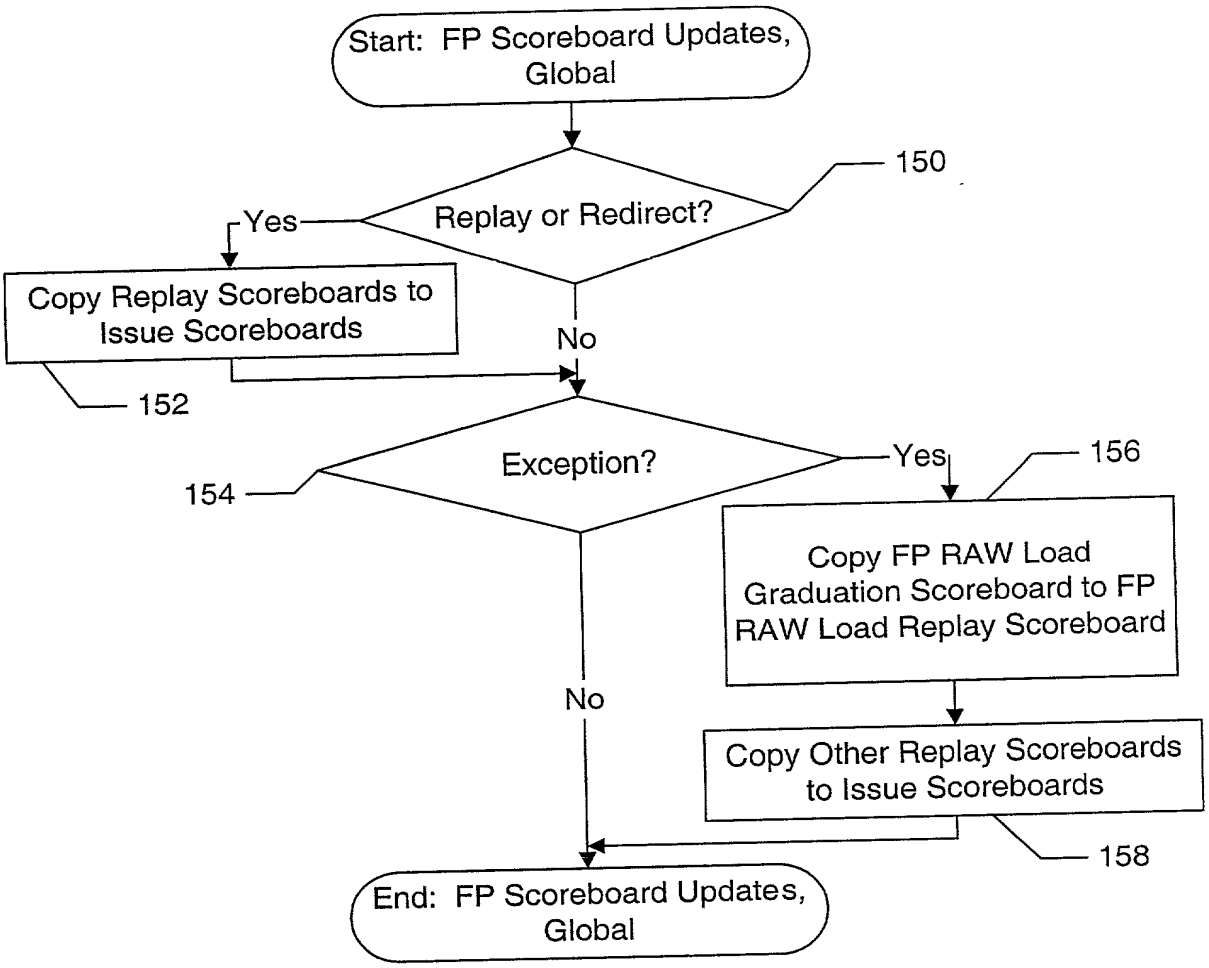
Start: FP Scoreboard Updates, Global
Replay or Redirect?
150
Yes
Copy Replay Scoreboards to Issue Scoreboards
152
No
Exception?
154
Yes
156
Copy FP RAW Load Graduation Scoreboard to FP RAW Load Replay Scoreboard
No
Copy Other Replay Scoreboards to Issue Scoreboards
158
End: FP Scoreboard Updates, Global

FIG. 12

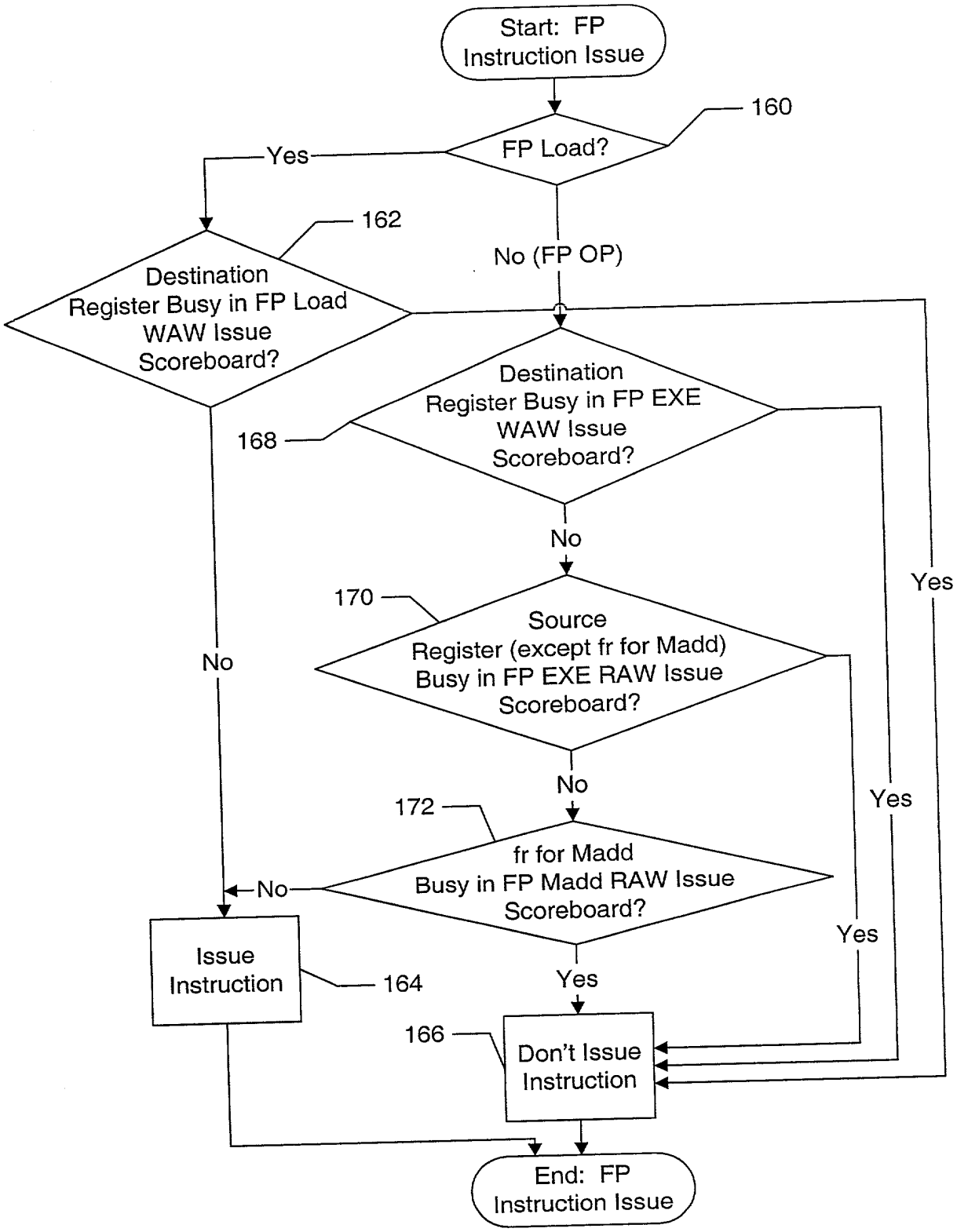
Start: FP Instruction Issue
160
FP Load?
Yes
No (FP OP)
162
Destination Register Busy in FP Load WAW Issue Scoreboard?
Destination Register Busy in FP EXE WAW Issue Scoreboard?
168
No
Yes
170
Source Register (except fr for Madd) Busy in FP EXE RAW Issue Scoreboard?
No
Yes
172
fr for Madd Busy in FP Madd RAW Issue Scoreboard?
No
Yes
Issue Instruction
164
Yes
166
Don't Issue Instruction
End: FP Instruction Issue

FIG. 13

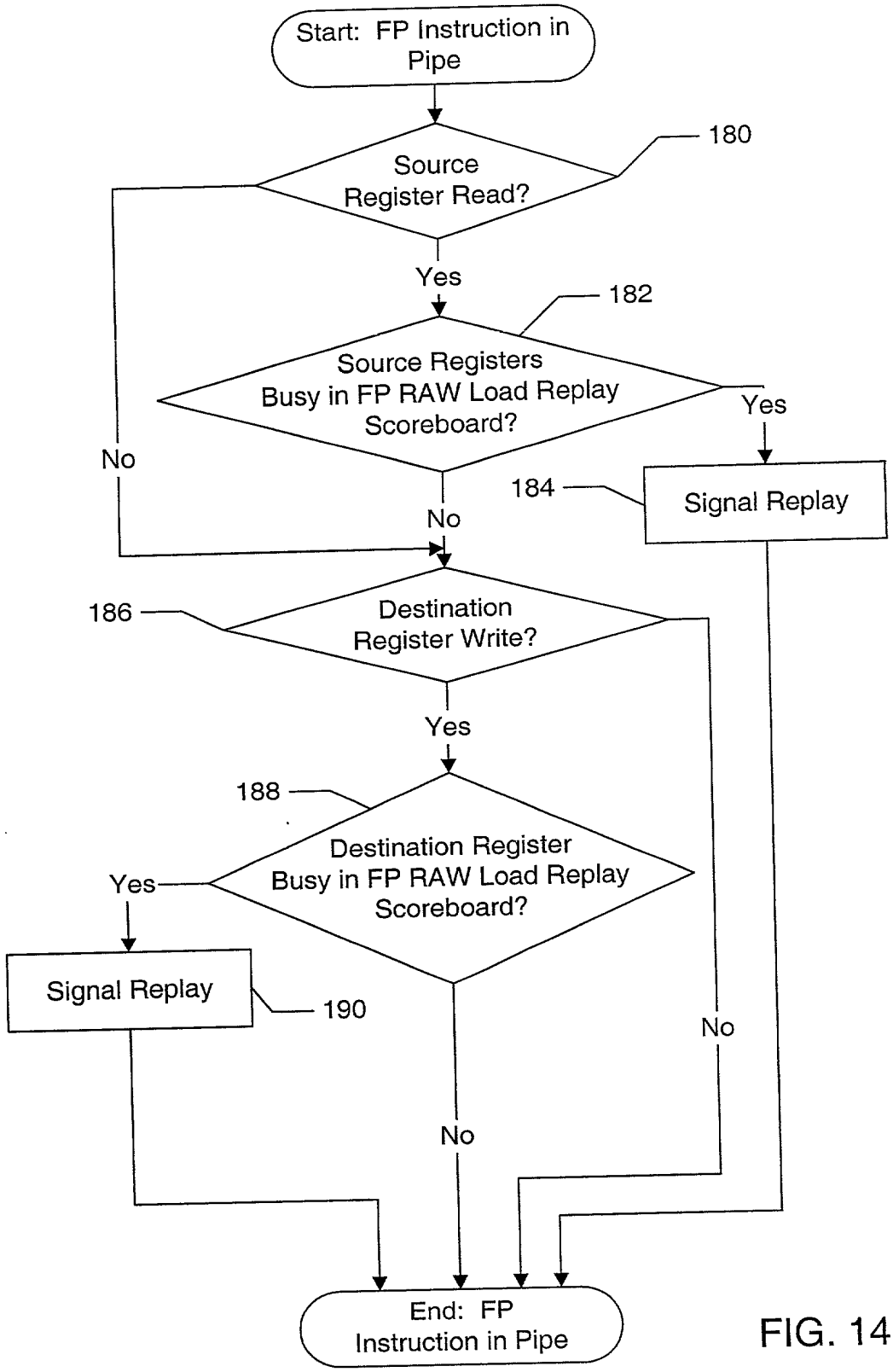
Start: FP Instruction in Pipe
Source Register Read?
180
Yes
No
182
Source Registers Busy in FP RAW Load Replay Scoreboard?
Yes
No
184
Signal Replay
186
Destination Register Write?
Yes
No
188
Destination Register Busy in FP RAW Load Replay Scoreboard?
Yes
No
Signal Replay
190
End: FP Instruction in Pipe

FIG. 14

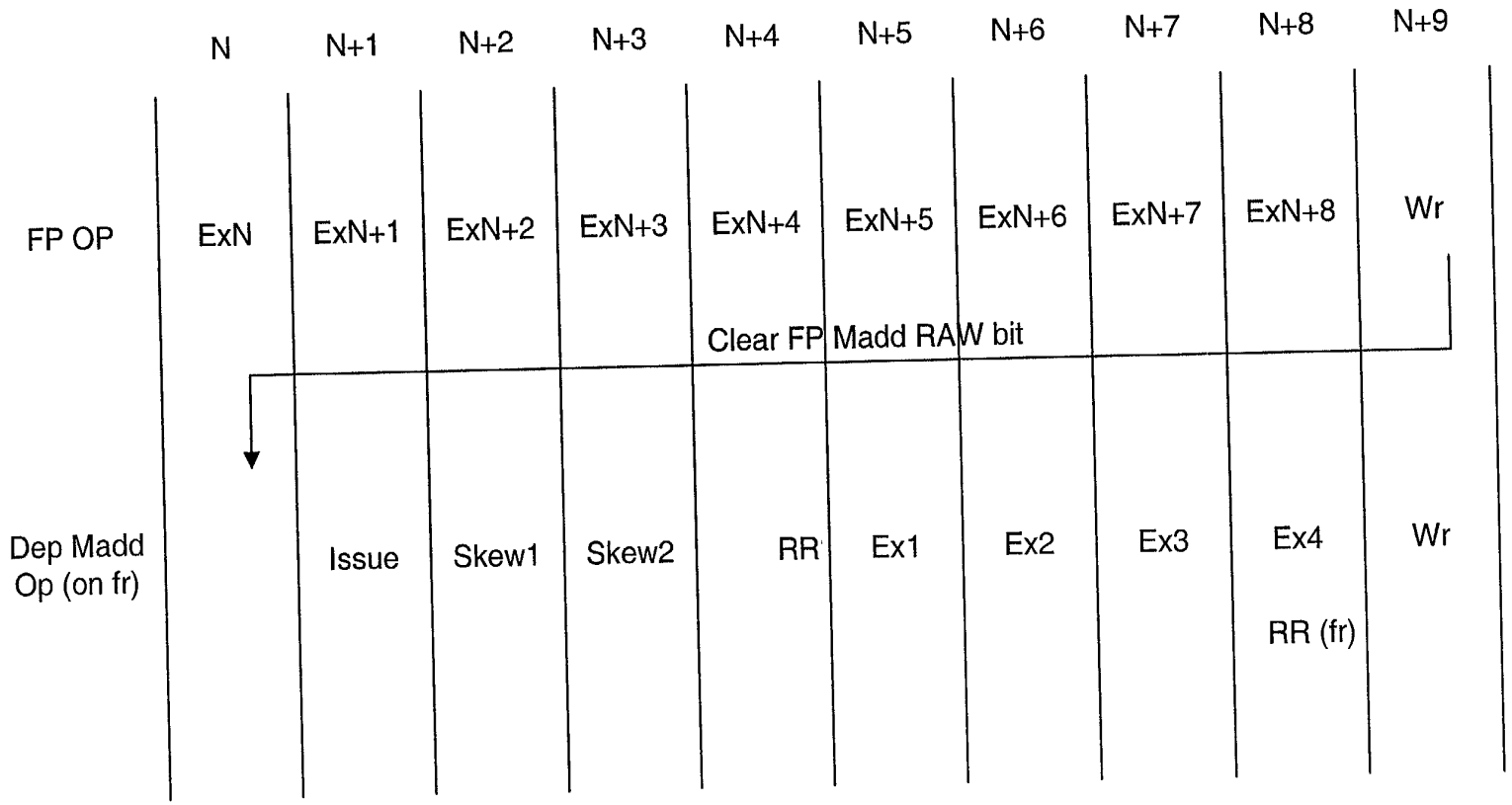

FIG. 15

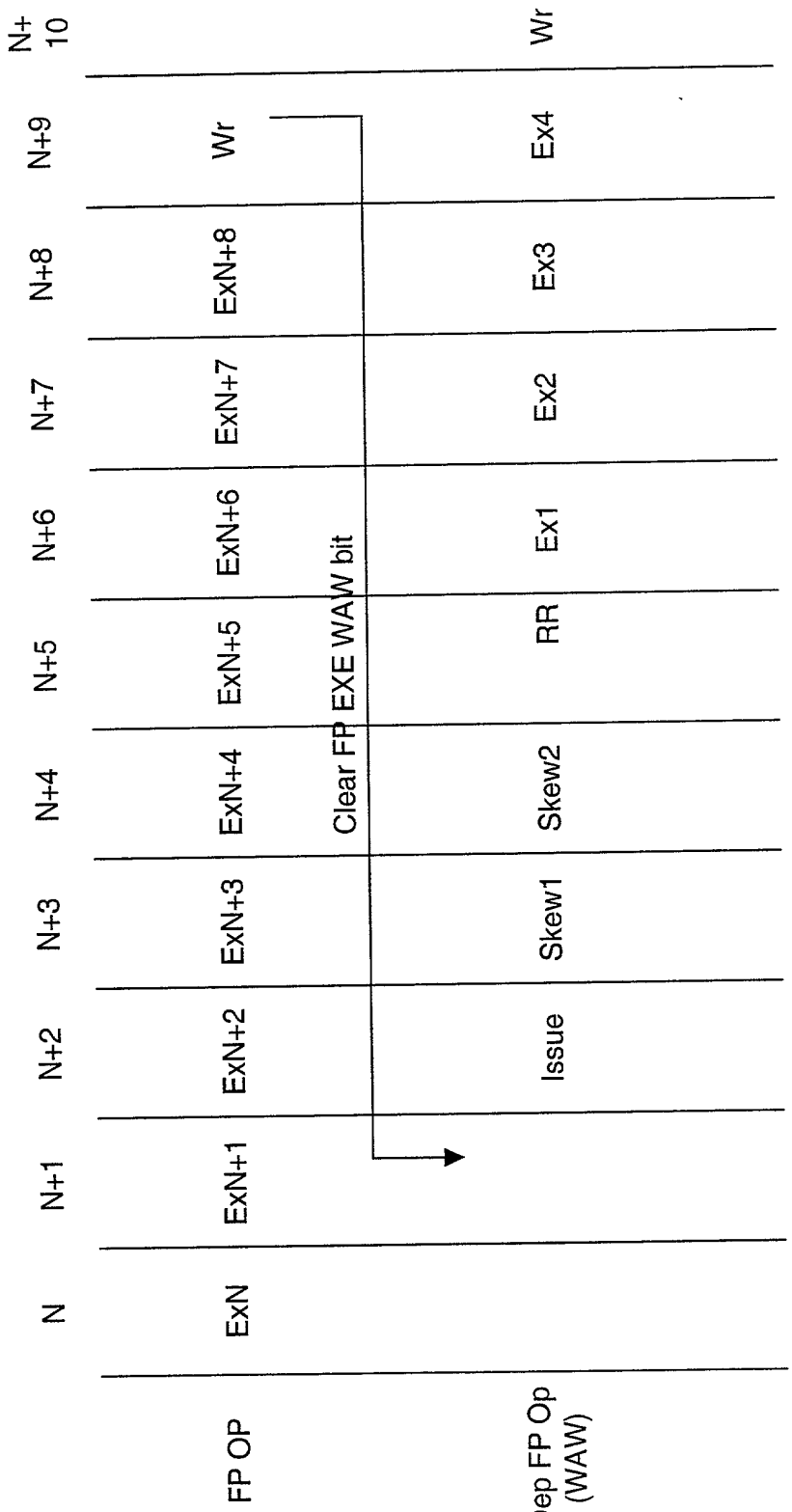
N
N+1
N+2
N+3
N+4
N+5
N+6
N+7
N+8
N+9
N+ 10
FP OP
ExN
ExN+1
ExN+2
ExN+3
ExN+4
ExN+5
ExN+6
ExN+7
ExN+8
Wr
Dep FP Op (WAW)
Issue
Skew1
Skew2
RR
Ex1
Ex2
Ex3
Ex4
Wr
Clear FP EXE WAW bit

FIG. 16

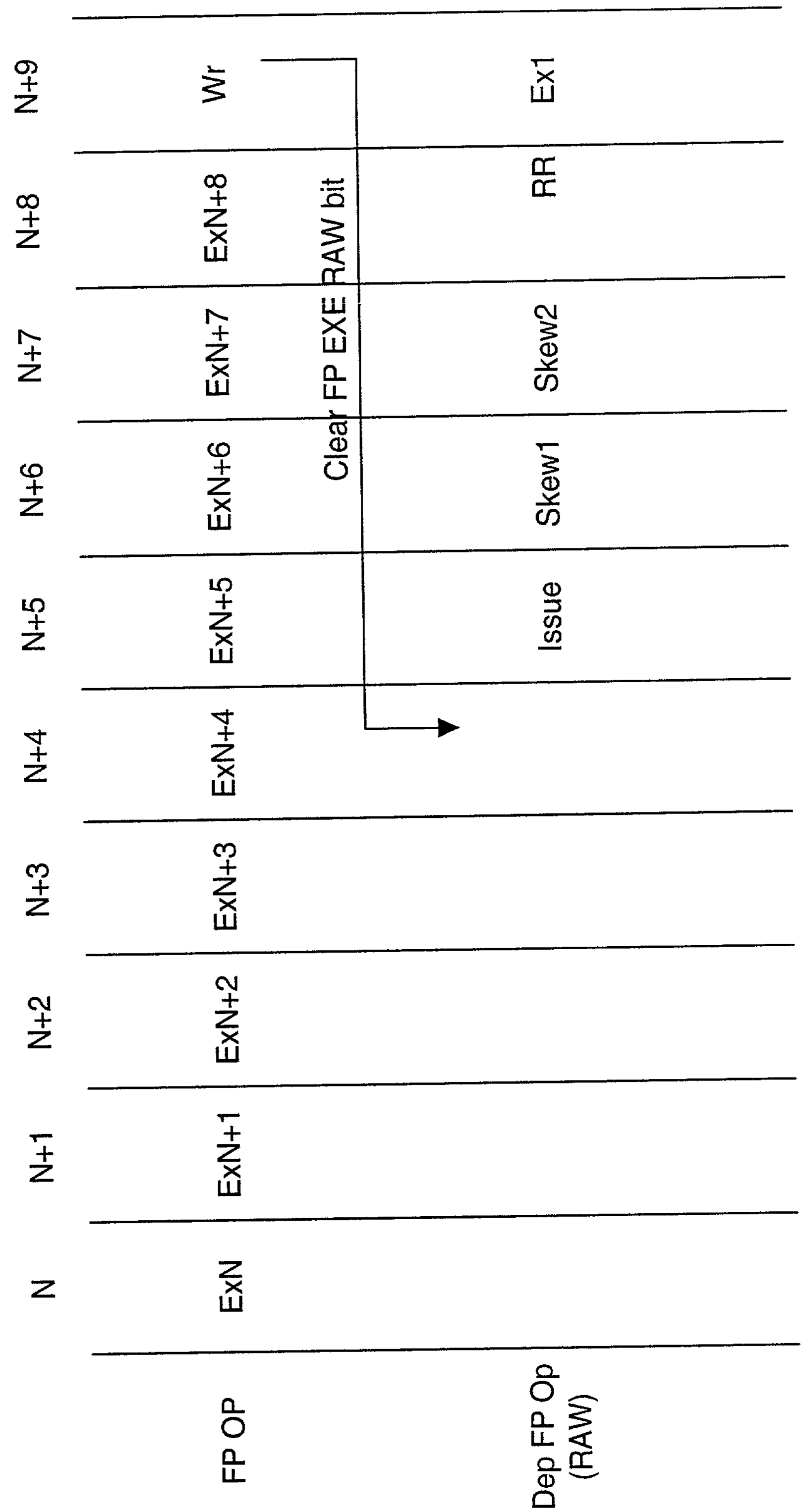
N
N+1
N+2
N+3
N+4
N+5
N+6
N+7
N+8
N+9
FP OP
ExN
ExN+1
ExN+2
ExN+3
ExN+4
ExN+5
ExN+6
ExN+7
ExN+8
Wr
Clear FP EXE RAW bit
Dep FP Op
(RAW)
Issue
Skew1
Skew2
RR
Ex1

FIG. 17.

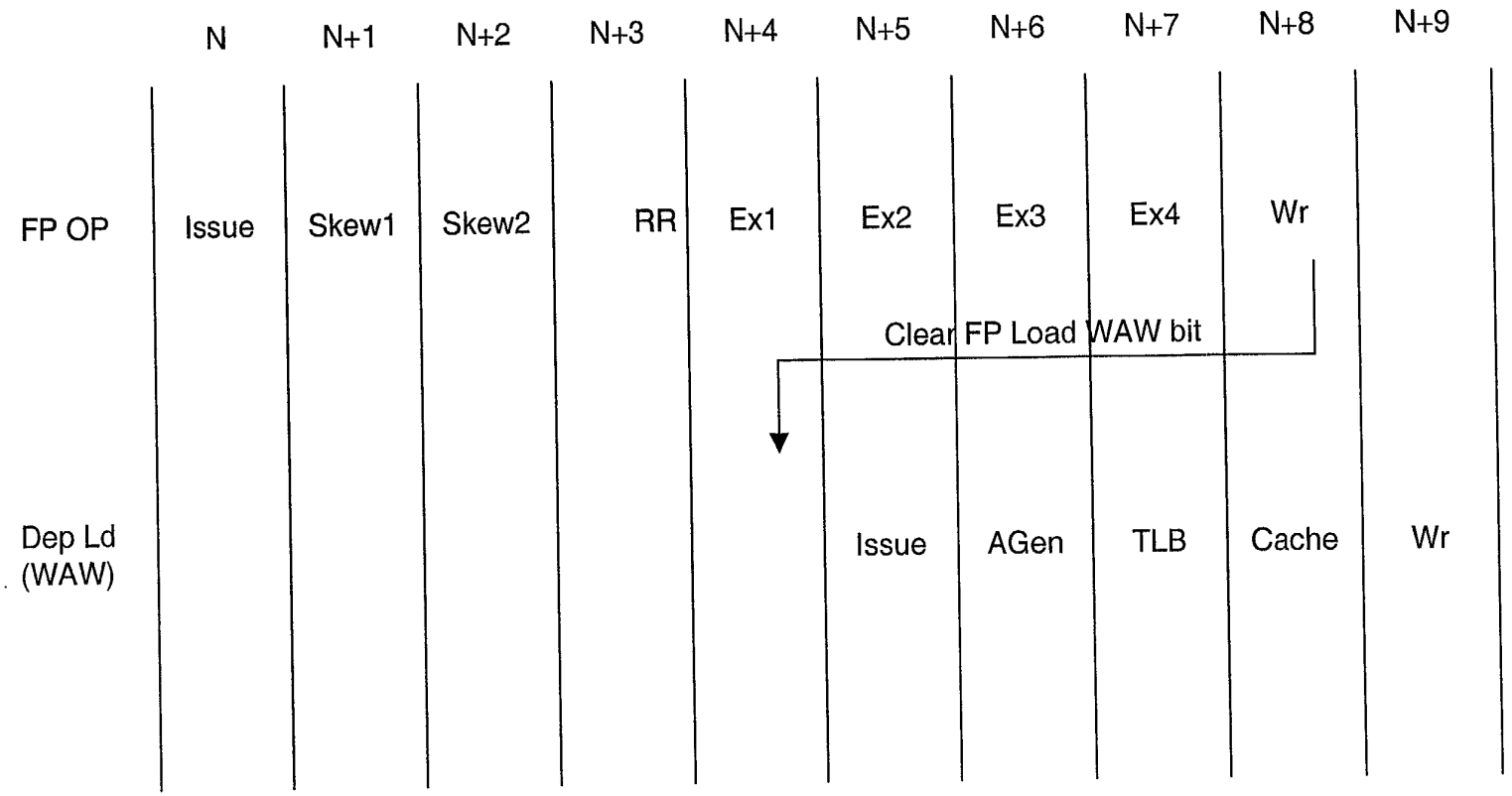

FIG. 18

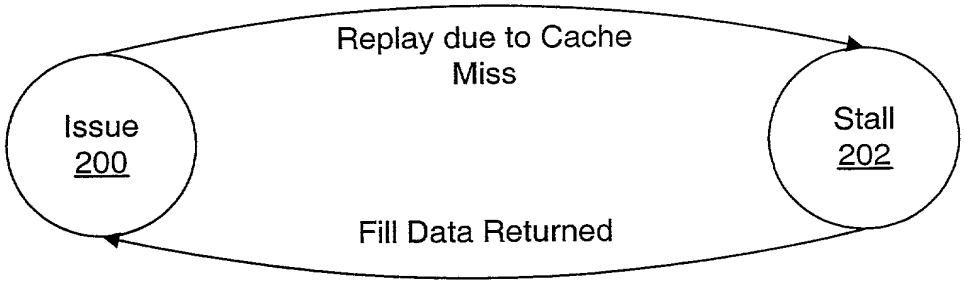
Replay due to Cache Miss
Issue 200
Stall 202
Fill Data Returned

FIG. 19

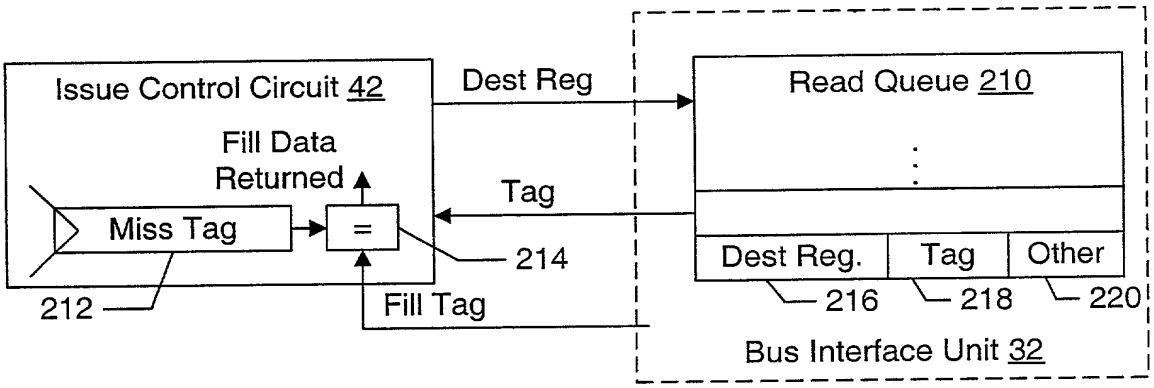
Issue Control Circuit 42
Dest Reg
Read Queue 210
Fill Data Returned
Tag
Miss Tag
=
214
Dest Reg.
Tag
Other
212
Fill Tag
216
218
220
Bus Interface Unit 32

FIG. 20

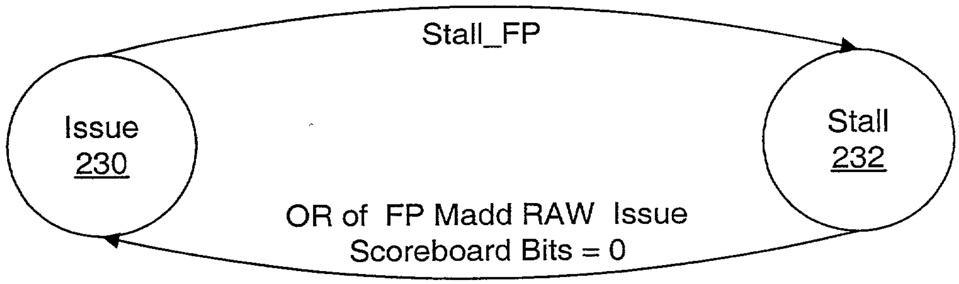
Stall_FP
Issue
230
Stall
232
OR of FP Madd RAW Issue
Scoreboard Bits = 0

FIG. 21

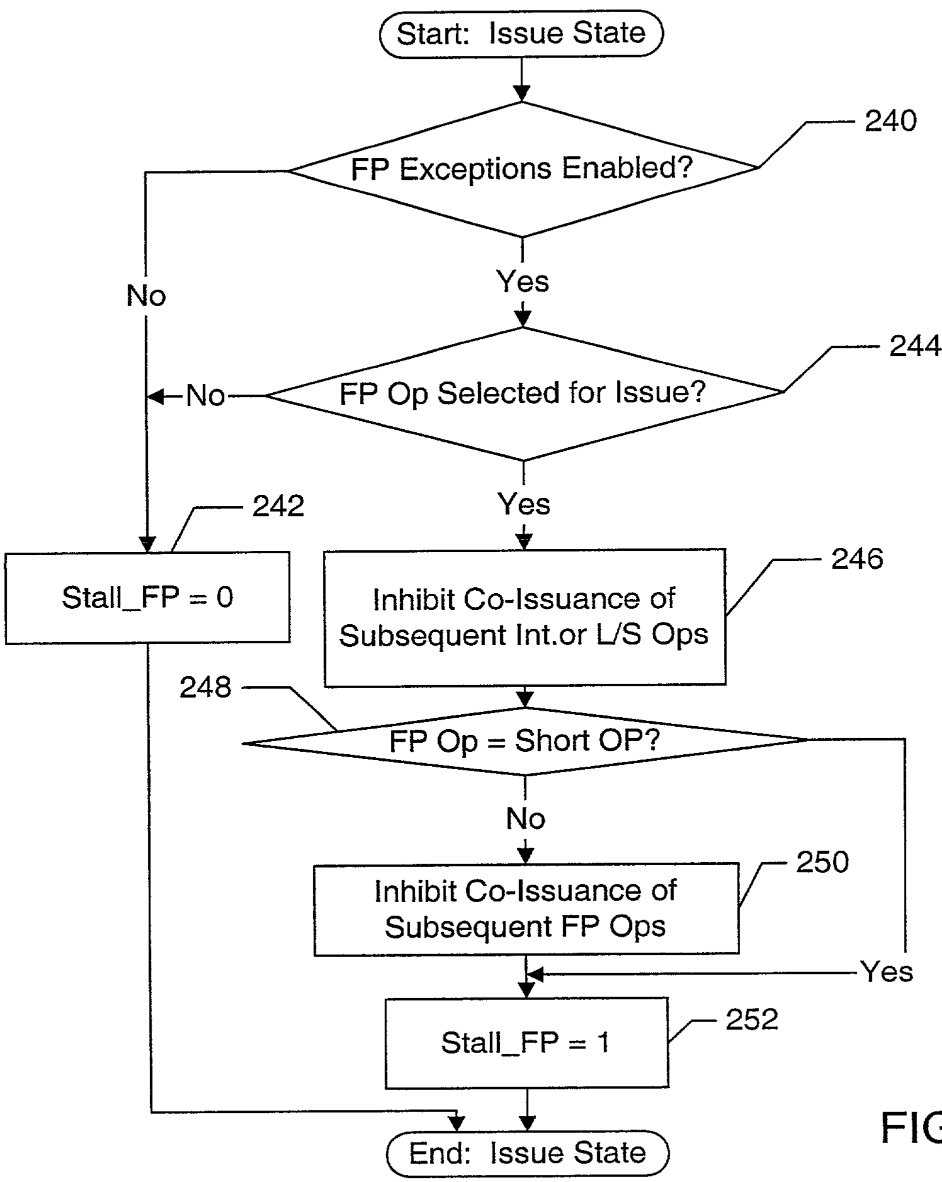
Start: Issue State
FP Exceptions Enabled?
240
No
Yes
FP Op Selected for Issue?
244
No
Yes
242
Stall_FP = 0
Inhibit Co-Issuance of
Subsequent Int.or L/S Ops
246
248
FP Op = Short OP?
No
Inhibit Co-Issuance of
Subsequent FP Ops
250
Yes
Stall_FP = 1
252
End: Issue State

FIG. 22

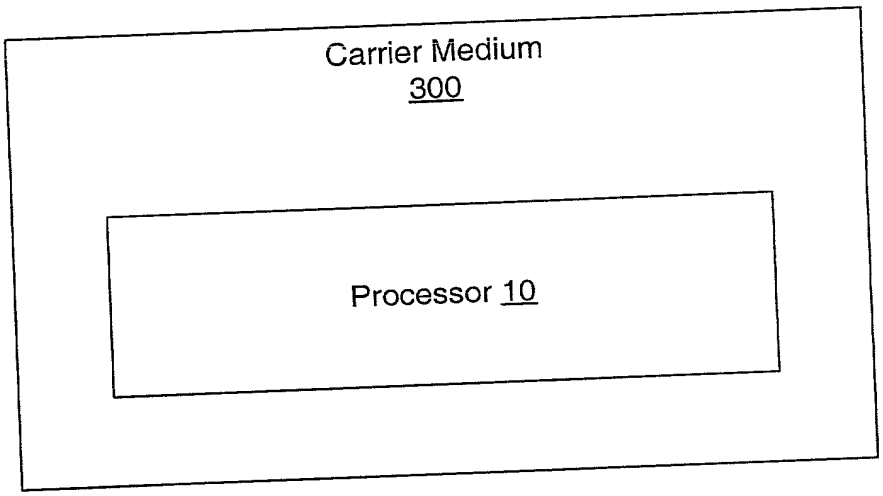

FIG. 23